PATENT
PD-8811FWC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	
MICHIO ASAHINA	ART GROUP UNIT: 2508
Serial No.: 07/780,455	EXAMINER: S. Loke
Filing Date: October 22, 1991	
For: SEMICONDUCTOR DEVICE	

AMENDMENT UNDER 37 C.F.R. § 1.116

Honorable Commissioner of
Patents & Trademarks
Washington, D.C. 20231

Dear Sir:

In response to the Examiner's Action dated January 4, 1993, kindly amend the above-identified application as follows:

IN THE CLAIMS:

Kindly cancel claim 26 and amend claim 25 as follows:

25. (AMENDED) A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region and a gate wiring, forming a lower conductor structure, and forming an insulating layer overlying said lower structure and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein each said step of forming a conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film; and

performing a plating operation in order to form a metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer; and

wherein said steps of forming a lower conductor structure and an upper conductor structure are carried out so that the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

Claim 28, line 12, after "one" insert -- conductor --.

REMARKS

The Examiner's Action dated January 4, 1993, has been received, and its contents carefully noted.

In order to advance prosecution, claim 26 has been placed in independent form by incorporation of its subject matter into parent claim 25.

The rejection of claims 26-28 as unpatentable over Hooper et al in view of Del Monte is respectfully traversed for the reason that the novel methods now defined in claim 25 (amended), 27 and 28 are not disclosed in or suggested by the teachings of the applied reference. Claim 25 now defines a method in which upper and lower conductor structures are each formed by forming at least one layer of a metal, etc, and then performing a plating operation in order to form a metal plating layer on the at least one layer, and in which the steps of forming the conductor structures are carried out

so that the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

Claim 27 defines the method according to the invention in which the plating operation is followed by a thermal treatment in order to diffuse material from the plating layer into the at least one layer of a metal, etc. As was previously pointed out, this results in a device in which projections 116 depicted in Figs. 1 and 2 are entirely avoided.

Claim 28 defines the method according to the invention in which the metal plating layer is deposited in openings formed in a patterned resist layer, after which the resist layer is removed and portions of the conductor layer underlying the plating layer are removed by etching, using the plating layer as a mask. As was previously pointed out, this represents an efficient method for giving the conductor structure a well defined configuration. The prior art now relied upon does not disclose any of the above-described features.

The newly cited reference, Hooper et al, describes a method in which two conductor structures are formed, each conductor structure including, as shown in Fig. 5 of the reference drawing, at least one metal layer 14, 18; 22, a copper layer 15; 23 formed by plating and a deposited molybdenum layer 16; 24. An insulating layer 20 overlies molybdenum layer 16. When comparing the structure shown in Fig. 5 of this reference with that formed by the method of claim 25, molybdenum layer 16 must be viewed as part of the lower conductor structure because claim 16 specifies that an insulating layer is formed to overlie the lower structure.

However, the method defined in claim 25 clearly differs from that disclosed in the applied reference because claim 25 specifies that the at least one layer of the upper conductor structure

contacts the metal plating layer. In the embodiment shown in Fig. 5 of the reference, the layer portions which can be equated to the at least one layer of the upper conductor structure contact an interposed molybdenum layer 16, rather than the plated layer 15. Thus, the method disclosed in this reference requires two deposition steps, for layers 16 and 24, in addition to those required by the method of claim 25, and the method disclosed in the reference will not be one in which a layer of the upper conductor structure contacts a metal plating layer. Thus, Hooper et al does not disclose the method defined in claim 25.

Clearly, Del Monte does not supply the teaching which is lacking from Hooper et al since Del Monte does not provide any disclosure of a method for forming two conductor structures which are separated from one another by an insulating layer.

As concerns claim 27, this specifies that the step of forming an upper conductor structure includes "after said step of performing a plating operation, performing a thermal treatment in order to diffuse material from the plating layer into the at least one layer". It is submitted that Hooper et al does not disclose this step. Recognizing this, the Examiner has relied on the disclosure appearing at column 11, lines 16-21 of Del Monte. Reliance on this portion of the Del Monte reference for this purpose does not appear appropriate since the disclosure in this portion of the reference indicates that sintering is to be avoided. In addition, this portion of the reference does not identify which of the layers would be sintering if sintering were not avoided. It is noted, in this connection, that the disclosure at column 11, lines 16-21 of Del Monte refers to the arrangement shown in Fig. 6, which includes, inter alia, a selected portion 14 of an interconnection network 79. It is further noted that the only

other disclosure in this reference which is directed to sintering is found at column 4, lines 54-65, which concerns sintering of the interconnection network material. In view of these elements of the disclosure of Del Monte, it can only fairly be concluded that Del Monte suggests the possibility of sintering material of the interconnection network 11 which is identified in the specification of Del Monte as being made of aluminum. No disclosure has been found in this reference of the method by which interconnection network 11 is formed.

Since Del Monte disclose that when a contact is formed to include a plated gold bump, sintering is to be avoided and, moreover, describes sintering only of an aluminum interconnection network, there is no basis for the conclusion that this reference discloses performing a thermal treatment in order to diffuse material from a plating layer into an underlying metal layer.

Claim 28 defines an aspect of the method according to the invention which results in a process simplification. Specifically, according to the method defined in claim 28, after forming at least one layer of a metal, etc, a patterned resist layer is formed on the at least one layer, a plating operation is performed in order to form a metal plating layer on the at least one layer, the patterned resist layer is removed, and portions of the at least one layer not covered by the plating layer are removed. In contrast, in the method disclosed by Hooper et al, and specifically at column 4, lines 13-27, an insulating layer 26 is deposited on molybdenum layer 14, a photoresist layer 28 is formed on the insulating layer 26 (and not on the conductor layer), the insulating layer is removed in regions which are not covered by the photoresist layer, the photoresist layer is removed while leaving the underlying insulating layer in place, the copper layer 30 is then formed by

plating, then the insulating layer is removed and the metal layer exposed by removal of the insulating layer is removed.

Thus, the method defined in claim 28 clearly distinguishes over that disclosed in the applied reference in that claim 28 includes the step of forming a patterned resist layer on a conductor layer and performing a plating operation in order to form a metal plating layer in the opening in the patterned resist layer, after which the patterned resist layer is removed. It will be noted that in the method disclosed in the applied reference, the photoresist layer is removed before formation of copper layer 30, which means, inter alia, that copper layer 30 cannot be formed in an opening in the patterned resist layer.

It should be readily apparent that the method disclosed in the applied reference includes the additional steps of first forming an insulating layer and then removing the insulating layer, both of which steps are avoided by the method defined in claim 28.

Accordingly, it is submitted that the claims remaining in the application clearly define patentably over any reasonable combination of the teachings of the applied references, and it is therefore requested that the remaining prior art rejection be reconsidered and withdrawn and that the application be allowed.

If for any reason, the Examiner finds the application in other than a condition for allowance, he is respectfully requested to call the undersigned attorney at the Washington, D.C. telephone number 223-5700 to discuss the steps necessary for placing the application in condition for allowance.

3/11/93
Date

Respectfully submitted,

Jay M. Finkelstein, 21,082

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on March 11, 1993.

Jay M. Finkelstein, Reg. No. 21,082

(signature) 3/11/93 (date)